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T. Bell
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Attorney's Docket No. 042390.P5769

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Gang Bai

Application No. 09/109,261

Filed: June 30, 1998

For: **A MULTI-LAYER GATE DIELECTRIC**

Examiner: Warren, M.

Art Group: 2815

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(A)
AND
AMENDMENT AND RESPONSE TO OFFICE ACTION

Box Amendments - Fee
Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

In accordance with 37 C.F.R. 1.136(a), the Applicant for the above-identified application respectfully petitions the Commissioner for a one (1) month extension of time, extending the period for response to May 30, 2001 from an outstanding Office Action dated January 31, 2001. The petition fee of $110.00 is submitted herewith. Please credit any overpayment or charge any additional amount due to Deposit Account 02-2666. A duplicate of the fee transmittal sheet is submitted herewith.

In response to the outstanding Office Action mailed January 31, 2001, Applicant respectfully requests consideration of the following remarks

REMARKS

Claims 8-21 were examined. No claim amendments are submitted. Claims 8-21 remain in the application.

A. 35 U.S.C. §103(a): Rejection of Claims 8-13 & 15-20

The Patent Office rejects claims 8-13 and 15-20 under 35 U.S.C. §103(a) as obvious over U.S. Patent No. 5,963,810 issued to Gardner et al. (Gardner) in view of U.S. Patent No. 4,015,281 issued to Nagata et al. (Nagata) and U.S. Patent No. 5,990,516 issued to Momose et al. (Momose).

The Patent Office cites Figure 3D of Gardner as showing a semiconductor device having a multi-layered gate dielectric. Gardner describes devices and techniques of fabricating devices having a nitrogen-enhanced relatively high permittivity or dielectric constant. The dielectric constant of the high permittivity gate insulator is typically greater than that of silicon dioxide (greater than 4.2). Col. 3, lines 21-23. Figures 3A-3D describe one fabrication process where nitride layer 303 of a layer thickness ranging from about 5 to 15 Å is formed followed by high permittivity layer 305. No technique is given for high permittivity layer 305.

In terms of thicknesses disclosed by Gardner, Applicant refers to the discussion in Gardner regarding Figures 2A-2C. In that fabrication process, Gardner describes a thickness of gate insulating layer 203 in the range from 100 to 3,000 Å. Col. 4, lines 2-3. Gardner recognizes that such thicknesses are substantially thicker than silicon dioxide gate dielectric thicknesses, but notes that the equivalent silicon dioxide thickness of insulating layer 203 can be less than a silicon dioxide gate dielectric. Col. 4, lines 3-8. An example is given of 1,000 Å of a PST oxide having a dielectric constant of about 3,000 equivalent to 1.4 Å of silicon dioxide having a dielectric constant of 0.2. Col. 4, lines 5-9. Gardner does not relate the gate dielectric thickness to gate lengths.

Momose describes a semiconductor device having a silicon dioxide gate dielectric. Momose describes forming single layer gate dielectrics less than 2.5 nm by carefully monitoring the heating temperature and time of a substrate. Momose also describes controlling gate lengths equal to a less than 0.3 μm.

Nagata is cited for describing a formula to determine the dielectric constant. Applicant's understanding of Nagata, however, is that it relates to isolation of adjacent devices.

Independent claim 8 is not obvious over the cited references, because the references fail to teach or provide any motivation for forming a transistor device having a gate dielectric wherein the gate dielectric thickness, t, is less than one-third of the length of the gate electrode with up to a dielectric constant, k, of $k_{ox}(t/t_{ox})$.

Gardner addresses multiple dielectric layers but notes the need to form substantially thicker dielectric layers than corresponding silicon dioxide gate dielectric. Gardner does this with the knowledge that its gate dielectric will have an equivalent oxide thickness (t_{ox}) less than conventional silicon dioxide gate electric layers. Momose teaches forming thin silicon dioxide gate dielectric, nothing further. The combined teachings of Gardner and Momose is that a substantially thicker multi-layer dielectric may have an equivalent silicon dioxide thickness less than the thin layers of Momose. Thus, one is left to speculate whether such multi-layer dielectric will be one-third the gate

length. Certainly no teaching or motivation to form it in such matter is presented. Gardner talks of equivalent oxide thickness as does Nagata. Neither talks of forming gate dielectrics less than one-third a length of a gate electrode. Such teachings cannot be found in Momose except for the fact that the structure formed with the silicon dioxide gate dielectric layer, meets such criteria. It does not follow from any of the references, that a non-silicon dioxide layer will have a gate dielectric thickness greater than one-third the gate length.

For the above stated reasons, claim 8 is not obvious over the cited references. Claims 9-13 depend from claim 8 and therefore contain all the limitations of that claim. For at least the reasons stated with respect to claim 8, claims 9-13 are not obvious over the cited references.

Independent claim 15 is not obvious over the cited references because, as noted above, the cited references fail to teach a multi-layer dielectric having a thickness, t, that is less than one-third a length of a gate electrode with up to a dielectric constant, k, of $k_{ox}(t/t_{ox})$. In this regard, as stated above, with respect to claim 8 are applicable here.

Claims 16-20 depend from claim 15 and therefore contain all the limitations of that claim. For at least the reasons stated with respect to claim 15, claims 16-20 are not obvious over the cited references.

Applicant respectfully requests the Patent Office withdraw the rejection to claims 8-13 and 15-20 under 35 U.S.C. §103(a).

B. 35 U.S.C. §103(a): Rejection of Claims 14 & 21

The Patent Office rejects claims 14 and 21 under 35 U.S.C. §103(a) as obvious over Gardner in view of Nagata and Momose and further in view of U.S. Patent No. 5,258,645 issued to Sato (Sato). Sato is cited for disclosing a tri-layered gate dielectric.

Claim 14 is dependent upon claim 8 and contain all the limitations of that claim. Claim 21 is dependent on claim 15 and contains all the limitations of that claim. For at least the reasons stated above, claims 14 and 21 are not obvious over the cited references. The fact that Sato discloses a tri-layered gate dielectric does not cure the defects noted above with respect to the independent claims.

Applicant respectfully requests that the Patent Office withdraw the rejection to claims 14 and 21 under 35 U.S.C. §103(a).

CONCLUSION

In view of the foregoing, it is believed that all claims now pending patentably define the subject invention over the prior art of record and are in condition for allowance and such action is earnestly solicited at the earliest possible date.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: 5/30/01

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on May 30, 2001.

Nedy Calderon 5/30/01

Nedy Calderon Date